Q.P. Code: 16MC802 **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

MCA I Year I Semester (R16) Supplementary Examinations June 2017

COMPUTER ORGANIZATION

(For Students admitted in 2016 only)

Time: 3 hours Max. Marks:60

(Answer all Five Units 5 X 12 = 60 Marks)

UNIT-I

1	a	Explain about half and full adder. Construct NAND and NOR gates with half-adder.	6M
	b	Explain the features of various types of flip-flops, with suitable illustrations.	6M

OR

2	a	What is mean by decoder and construct a 2x4 decoder.	6M
	b	Write a 4-bit gray code, give the advantages and applications of gray code.	6M

UNIT-II

3		What is the importance of cache memory and briefly explain the types of memory mapping.	12M

OR

4		Briefly explain the design of control unit.	12M

UNIT-III

5	a	Explain about the assembler directives.	7M
	b	Describe Data Transfer	5M

OR

6		Explain about addressing modes. With example	12M

UNIT-IV

7	a	Write a short notes on:Programmed I/O	6M
	b	Wrie a short notes on Interrupt - initiated I/O	6M

OR

8		What is DMA? Explain DMA controller with a block diagram.	12M

UNIT-V

9		What is pipeline processing? Explain Instruction Pipelining with example.	12M

OR

10		Explain about inter processor arbitration techniques.	12M

***** END *****